

What is claimed is:

1 1. A method for performing an on-board test of
2 connections between two programmable array circuits,
3 comprising the steps of:

4 disposing a first connection circuit on a first
5 programmable array circuit according to a preset
6 linear feedback shift register (LFSR) polynomial;

7 disposing a second connection circuit on a second
8 programmable array circuit according to the
9 preset LFSR polynomial, wherein the second
10 connection circuit has a shift register and
11 wherein pins of the second connection circuit are
12 connected to the corresponding pins of the first
13 connection circuit;

14 inputting a test pattern to the shift register, wherein
15 the test pattern is processed by the shift
16 register circuit and wherein a particular pattern
17 is produced from an output pin of the shift
18 register; and

19 examining the particular pattern to acquire a
20 connection status of the first and the second
21 connection circuits.

1 2. The method as claimed in claim 1, wherein the
2 shift register comprises a plurality of D-type flip-flops
3 connected in serial.

1 3. The method as claimed in claim 1, wherein a
2 plurality of XOR gates are disposed in the first connection
3 circuit when an LFSR circuit with the XOR gates outside the

4 shift register is used to achieve the preset LFSR
5 polynomial.

1 4. The method as claimed in claim 1, wherein a
2 plurality of XOR gates are disposed in the second connection
3 circuit when an LFSR circuit with the XOR gates inside the
4 shift register is used to achieve the preset LFSR
5 polynomial.

1 5. The method as claimed in claim 1, wherein the test
2 pattern and the particular pattern are related in the form
3 of a polynomial.

1 6. The method as claimed in claim 1, wherein the
2 status includes bus speed and an appearance of cross talk.

1 7. The method as claimed in claim 1, wherein the
2 programmable arrays circuits are FPGAs.

3 8. A circuit for performing an on-board test of
4 connections between two programmable arrays circuits,
5 comprising:

6 a first connection circuit connected with a first
7 programmable arrays circuit; and

8 a second connection circuit having a shift register and
9 connected between the first connection circuit
10 and a second programmable arrays circuit,

11 wherein the first and the second connection circuits
12 are disposed according to a preset linear
13 feedback shift register (LFSR) polynomial,
14 wherein a test pattern is input to and processed
15 by the shift register, and then a particular

16 pattern is produced from an output pin of the
17 shift register, and wherein the particular
18 pattern is examined to acquire a connection
19 status of the first and the second connection
20 circuits.

1 9. The method as claimed in claim 8, wherein the
2 shift register comprises a plurality of D-type flip-flops
3 connected in serial.

1 10. The method as claimed in claim 8, wherein the
2 first connection circuit has a plurality of XOR gates when
3 an LFSR circuit with the XOR gates outside the shift
4 register is used to achieve the preset LFSR polynomial.

1 11. The method as claimed in claim 8, wherein the
2 second connection circuit has a plurality of XOR gates when
3 an LFSR circuit with the XOR gates inside the shift register
4 is used to achieve the preset LFSR polynomial.

1 12. The method as claimed in claim 8, wherein the test
2 pattern and the particular pattern are related in the form
3 of a polynomial.

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5 13. The method as claimed in claim 8, wherein the
6 programmable arrays circuits are FPGAs.